## REMARKS/ARGUMENTS

Amendments were made to the specification. No new matter has been added by any of the amendments to the specification.

Claims 1, 3, 4, 6-10, 12, 13, 15-17, and 19-28 are pending in the present application. Claims 2, 5, 11, 14, and 18 are canceled. Claims 1, 3, 4, 7-10, 12, 13, 16, 17, 19, 20, and 23 are amended. Claims 24-28 are added. The amendments to these claims correct typographical errors and address the objections, the indefiniteness rejections, and the statutory subject matter rejections. Support for the amendments to the claims can be found in the claims as originally filed and in the specification on page 24, lines 1-19. Claims 24-28 are added. Claims 24-28 are added to further specify in the independent claims that the partitions comprise logical partitioned data processing systems. Support for the new claims can be found in the specification on page 1, lines 18-26; page 6, lines 21-25; and page 20, lines 1-10.

### I. Examiner Interview

On June 9, 2006, the examiner and the undersigned attorney discussed the rejection under 35 U.S.C. § 101 and the rejection of claim 1 under 35 U.S.C. § 102. An agreement was reached to amend the claims to overcome the rejections under 35 U.S.C. § 101. No agreement was reached regarding the rejections under 35 U.S.C. § 102.

### II. Objection to the Specification

The examiner objects to the specification under the assertion that the docket number should be removed from the abstract. Applicants have amended the specification accordingly. Applicants have also amended the abstract to correct a typographical error.

### III. Objections to the Claims

The examiner objects to claims 2, 3, 8, 11, 12, 18, and 19 under the assertion that these claims contain informalities enumerated on page 3 of the office action of March 17, 2006. The objection to claims 2, 11, and 18 are moot as these claims have been canceled. Applicants have amended the remaining claims accordingly.

### IV. Rejections Under 35 U.S.C. § 112, Second Paragraph

The examiner rejected claims 1-23 as indefinite for the reasons enumerated on pages 3 through 4 of the office action of March 17, 2006. The rejection with respect to claims 2, 5, 11, 14, and 18 is moot as these claims have been canceled. Applicants have amended the remaining claims accordingly.



PAGE 10/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

V. Rejections Under 35 U.S.C. § 101

The examiner rejected claims 17-23 under the assertion that these claims are directed to non-statutory subject matter. The rejection with respect to claim 18 is moot as this claim has been canceled. Without admitting that the claims as-filed were non-statutory, Applicants have amended the claims accordingly.

VI. 35 U.S.C. § 102, Anticipation

VI.A. Claims 1, 4, and 8

The examiner rejected claims 1, 4, 8, 10, and 13 under 35 U.S.C. § 102(e) as anticipated by *Olarig et al.*, Dynamic Cache Partitioning, U.S. Patent Application Publication 2003/0065886 (April 3, 2003). This rejection is respectfully traversed.

Regarding claim 1, the examiner states that:

> As for claims 1, 8 and 10, Olarig teaches a method (and system) for assigning processors to partitions in a multi-processor data processing system, the method comprising:
>
> generating optimal allocation sets for unallocated processors in the multiprocessor data processing system for a cache level, wherein each set includes an allocation of unallocated processors to at least one partition (the cache can be partitioned variety of different manners in order to optimize the processors' utilization of the cache memory. For example, each of the eight processors may have their own unique partition of the cache if needed to optimize allocation - paragraph 0019, all lines. Note the processors are unallocated until a determination is made as to which processors are to be allocated to their respective cache partitions);
>
> determining whether a set in the optimal allocation sets match requirements for a set of partitions selected for the data processing system (cache optimization can be determined based on cache utilization - paragraph 0021, all lines. In other words, if a running hit average of the cache hits a certain value; the partitions can be allocated to processors in order to optimize the system's efficiency. The system checks to see if the parameters are met or matched to make the determination); and
>
> responsive to a match existing, removing processors in the set from the unallocated processors, wherein cache usage by the processors is optimized for the cache level (paragraph 0021, all lines - again the cache will be repartitioned based on the statistics previously calculated for system efficiency. It is also worthy to note that the system is not just limited in resizing the previous partitions, but it is also capable of reallocating the cache partitions based on the statistical information. This way, the system can assign processors to partitions in order to optimize the system for that cache level - see paragraphs 0026 and 0027, all lines).



PAGE 11/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

Office Action of March 17, 2006, pp. 5-7

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims.

Claim 1 as amended is as follows:

> 1. A method for assigning processors to partitions in a multi-processor data processing system, the method comprising:
>
> generating optimal allocation sets for unallocated processors in the multi-processor data processing system for a cache level, wherein each optimal allocation set includes an allocation of unallocated processors to at least one partition;
>
> determining whether a first set in the optimal allocation sets matches requirements for a set of partitions selected for the data processing system; and
>
> responsive to a match existing, removing processors in the first set from the unallocated processors to form a group of removed processors, wherein cache usage by the group of removed processors is optimized for the cache level.

*Olarig* does not anticipate claim 1 because *Olarig* does not show any of the features of claim 1. As shown below, the examiner's assertions to the contrary are incorrect. Therefore, *Olarig* does not anticipate claim 1.

Nevertheless, the examiner asserts that *Olarig* teaches the claimed feature of "generating optimal allocation sets for unallocated processors in the multi-processor data processing system for a cache level, wherein each optimal allocation set includes an allocation of unallocated processors to at least one partition." The examiner cites the following portion of *Olarig* to support this assertion:

> [0019] Any of caches 120, 126 and 140 can be partitioned into cache portions or bins which behave as multiple caches. Cache address space is divided among these cache partitions. Each cache partition of the cache 120, 126 or 140 can be assigned a different logical or physical entity. For example, the cache 120 can be partitioned into two cache bins with one cache bin dedicated to the processor bus 160 and the other cache bin dedicated to the processor bus 162. Alternatively, the cache 120 can be partitioned into eight bins with each bin dedicated to a different processor of the processors 102-116. As another example, the cache 140 can be partitioned into four bins with each bin dedicated to a different PCI resource of the PCI resources 142-148. Other examples of entities that can be allocated dedicated cache partitions include processes, threads and nodes. It should be



PAGE 12/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

> understood that this list is only illustrative and not exhaustive of the many types of entities present or supported within a computer system.

*Olarig*, paragraph 19.

*Olarig* teaches that *caches* can be partitioned into cache portions or bins. Each bin is assigned to a different logical entity, such as an operation system thread, or to physical entity, such as a processor bus or a processor. In contrast, claim 1 requires that, "each optimal allocation set includes an *allocation of unallocated processors to at least one partition*."

When *Olarig's* teachings and the claimed features are compared, one can see that the examiner's understanding of *Olarig* vis-à-vis claim 1 is backwards. *Olarig* partitions caches and then assigns the partitions of caches to processors. In contrast, claim 1 requires an allocation of unallocated processors *to at least one partition*. Therefore, *Olarig* teachings are opposite to the claimed feature. For this reason, *Olarig* does not teach the claimed feature.

Additionally, *Olarig* does not teach the claimed feature of "generating optimal allocation sets." Nothing in the cited portion of *Olarig* or in other portions of *Olarig* teaches this claimed feature. For example, nothing in *Olarig* teaches or suggests that assigning eight cache bins to eight processors is an optimal allocation. Similarly, nothing in *Olarig* teaches or suggests that optimal allocation sets for *unallocated processors* are generated. Instead, *Olarig* only teaches assigning *cache partitions* to processors. Therefore, assuming *arguendo* that *Olarig* generates optimal allocation sets, the sets are for *unallocated cache partitions* and not for *unallocated processors*, as claimed. For this reason, *Olarig* does not teach the claimed feature.

In addition, *Olarig* does not teach the claimed feature of "determining whether a first set in the optimal allocation sets matches requirements for a set of partitions selected for the data processing system." The examiner asserts otherwise, citing the following portion of *Olarig*:

> [0021] While a partitioned cache represents one form of cache optimization, a partitioned cache can be further optimized by reallocating the sizes of cache partitions based on the activity of the particular cache partitions. One cache statistic that may be useful in identifying cache partitions that are candidates for size reallocation is a moving or running hit average. This cache statistic represents an average number of hits to a cache partition over a particular period of time. Referring to FIG. 2, an exemplary moving hit average calculation technique is shown. This technique can be performed in parallel by a cache controller for each cache partition of its cache. Beginning in step 200, the t variable representing time is set to zero. Next, in step 202, a hit counter HIT_CNT[i] is set to zero. The i variable is an index used to represent a particular cache partition.

*Olarig*, paragraph 21.



PAGE 13/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

This portion of *Olarig* teaches that cache partitions can be optimized by reallocating the size of cache partitions. The "running hit average" is a metric used for identifying which cache partitions are candidates for size reallocation.

In contrast, claim 1 requires determining whether a first set in the optimal allocation sets matches requirements for a set of partitions. In the context of the rest of claim 1, the term "optimal allocation sets" includes "unallocated *processors*." Therefore, while *Olarig* teaches optimization of *cache* partitions, claim 1 requires determining whether a first set in the optimal allocation sets of unallocated processors matches requirements for a set of partitions. When directly compared, the stark contrast between *Olarig* and the feature of claim 1 is apparent. Moreover, nothing else in *Olarig* teaches this claimed feature.

In addition, *Olarig* does not teach the claimed feature of, "responsive to a match existing, removing processors in the first set from the unallocated processors to form a group of removed processors, wherein cache usage by the group of removed processors is optimized for the cache level." The examiner asserts otherwise, citing paragraph 21 of *Olarig* and the following additional portions of *Olarig*:

> [0026] Steps 302 and 306 together define the reallocation criteria for identifying cache partitions as reallocation candidates. This exemplary choice of reallocation criteria depends on the behavior of at least two cache partitions where one cache partition is trending higher and another cache partition is trending lower. By not focusing strictly on the trend for one cache partition, the size of one cache partition is not optimized at the expense of the size of another cache partition. Instead, the process optimizes the size allocation of each cache partition. Size reallocation for cache partitions presents a flexible cache solution for minimizing cache thrashing. A further advantage is that the organization of the partitioned cache dynamically adapts to the current trend or activity of the cache partitions.
>
> [0027] Reallocation criteria for identifying cache partitions as reallocation candidates can be determined in a variety of ways. One way is for the user to pre-define the criteria. This criteria may or may not filter transient-based behavior. Another approach is for trace data to be captured and studied such that criteria are selected based on performance analysis. Similarly, reallocation schemes can be employed in a variety of ways. One sophisticated approach can involve a searching or tracking algorithm for locating certain trends or "hot spot" activity in behavior of the cache partitions. In this context, "hot spot" activity generally refers to an area in a computer system with frequent cache activity, suggesting a larger cache partition for that area would be helpful. A couple of factors worth considering in choosing a reallocation scheme are ease of implementation in hardware and ease of testing.

*Olarig*, paragraphs 26 and 27.

As shown above, paragraph 21 of *Olarig* teaches optimizing cache partitions by reallocating the sizes of the cache partitions relative to the workload of the cache partitions. Paragraphs 26 and 27 of



PAGE 14/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

*Olarig* teach other cache reallocation criteria for reallocating the sizes of the cache partitions. These paragraphs also teach methods for determining cache reallocation criteria.

However, none of the cited portions of *Olarig* teach removing *processors* from the unallocated processors, wherein cache usage by the group of removed processors is optimized for the cache *level*, as claimed in claim 1. As shown above, *Olarig* does not remove processors from unallocated processors, as claimed in claim 1. Instead, at best, *Olarig* teaches removing caches from unallocated caches. Furthermore, nothing in the cited portions of *Olarig* teaches that the group of remove processors is optimized for a cache *level*, as claimed in claim 1. Instead, *Olarig* is unconcerned with the level of the cache being partitioned. Note, for example, that in the background *Olarig* discusses the existence of cache levels but then fails to treat cache levels with respect to his technique. Therefore, *Olarig* does not teach this feature of claim 1.

As shown above, *Olarig* does not teach any of the features of claim 1. Therefore, *Olarig* does not anticipate claim 1.

Claim 4 depends from claim 1. *Olarig* does not anticipate claim 4 at least by virtue of the dependence of claim 8 on claim 1. Furthermore, nothing in *Olarig* teaches "removing a partition from the set of partitions in response to allocating the first set [in the optimal allocation sets of unallocated processors] to the partition," as claimed in claim 4. Therefore, *Olarig* does not anticipate claim 4.

Claim 8 contains features similar to those presented in claim 1. Therefore, *Olarig* does not anticipate claim 8 at least for the reasons presented vis-à-vis claim 1.

**VI.B. Claims 24-28**

New claims 24-28 depend from the rejected independent claims. Therefore, *Olarig* does not anticipate claims 24-28 at least for the reasons described above vis-à-vis claim 1.

In addition, new claims 24-28 further specify that the partitions comprise logical partitioned data processing systems. As described above, *Olarig* teaches partitioning *caches* and assigning cache partitions to processors and other entities. However, for example, *Olarig* does not teach that "each set includes an allocation of unallocated processors to at least one *logical partitioned data processing system*," as claimed in claim 24. *Olarig* does not teach determining whether a first set in the optimal allocation sets matches requirements for a set of *logical partitioned data processing systems*," as claimed in claim 24. Therefore, *Olarig* does not anticipate claim 24. For similar reasons, because claims 25-28 contain similar features Olarig does not anticipate claims 25-28.



PAGE 15/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

**VI.C. Conclusion as to the Anticipation Rejection**

*Olarig* does not anticipate the claims because *Olarig* does not teach all of the features of the claims, as explained above. Furthermore, *Olarig* does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. Absent the examiner pointing out some teaching or incentive to implement *Olarig* and allocating processors to partitions or logical partitioned data processing systems, one of ordinary skill in the art would not be led to modify *Olarig* to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify *Olarig* in this manner, the presently claimed invention can be reached only through an improper use of hindsight using Applicants' disclosure as a template to make the necessary changes to reach the claimed invention.

**VII. 35 U.S.C. § 103, Obviousness**

**VII.A. Claims 2, 3, 11, and 12**

The examiner rejected claims 2, 3, 11, and 12 under 35 U.S.C. § 103 as obvious over *Olarig* in view of *Arimilli et al.*, Eviction Override for Larx-Reserved Addresses, U.S. Patent 6,212,605 (April 3, 2001) (hereinafter "*Arimilli '605*"). The rejection is moot with respect to claims 2 and 11 as these claims have been canceled. However, Applicants point out that the features of claim 2 have been incorporated into claim 3 and the features of claim 11 have been incorporated into claim 12. With respect to claims 3 and 12 this rejection is respectfully traversed. The examiner states that:

> As for claim 2-3 and 11-12, though Olarig teaches his system as including multiple cache levels, he fails to teach repeating the steps of claim 1 (and claim 10) for each cache level by moving from the highest cache level, to each successively lower cache level.
>
> Arimilli '605 however teaches a method for controlling eviction of cache blocks to override the eviction of a value, which is reserved for a later operation. More specifically, Arimilli '605 teaches performing system operations on a hierarchical, multilevel cache (i.e. setting an address reservation flag), by starting at the highest cache level (in this case, L2), and then repeating the system operation on the next lower level - col. 3, lines 46-65.
>
> It would have been obvious to one of ordinary skill in the art at the time of the invention for Olarig to further include Arimilli's ('605) system of eviction override into his own system of cache partitioning, in order to facilitate repeating the partitioning/allocation techniques of his memory system on each successive level of cache. By doing so, Olarig would benefit by having a means of improving the overall processor performance of his system by avoiding unnecessary evictions to the cache. This way the overall performance will improve, by avoiding a scenario in which a block that has be unnecessarily evicted must be reloaded into the cache as taught by Arimilli '605 - col. 7, lines 38-58.



PAGE 16/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

Office Action of March 17, 2006, p.8.

If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985). A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994).

The examiner has failed to state a *prima facie* obviousness rejection of claims 3 and 12 because the proposed combination, when considered as a whole, does not teach all of the features of these claims. As shown above vis-à-vis the response to the anticipation rejection of claim 1, *Olarig* does not teach any of the claimed features of independent claims 1 and 10, from which claims 3 and 12 depend. Additionally, *Olarig* does not suggest any of the features of these claims because *Olarig's* teachings deal with partitioning caches and assigning the cache partitions to processors or other entities, not to assigning processors to partitions as claimed in these claims.

Moreover, *Arimilli '605* does not teach or suggest any of the features of claim 1 or of claim 10. *Arimilli '605* is directed to a method of controlling eviction of cache blocks to override eviction of a value which is reserved for a later operation. Nothing in *Arimilli '605* teaches or suggests assigning processors to partitions, as claimed, or that cache usage by the processors is optimized for the cache level, as claimed in these claims.

Because neither *Arimilli '605* nor *Olarig* teach or suggest all of the features of claim 1 or of claim 10, the proposed combination of *Arimilli '605* and *Olarig*, when considered as a whole, does not teach or suggest all of the features of claim 1 or of claim 10. Therefore, under the standards of *In re Lowry* and *In re Grabiak*, the examiner has failed to state a *prima facie* obviousness rejection of claims 3 and 12.

**VII.B. Claims 5-7 and 14-16**

The examiner rejected claims 5-7 and 14-16 under 35 U.S.C. § 103 as obvious over *Olarig* in view of *Arimilli et al.*, Data Processing System with Configurable Memory Bus and Scalability Ports, U.S. Patent 6,581,115 (June 17, 2003) (hereinafter "*Arimilli '115*"). The rejection is moot with respect to claims 5 and 14, as these claims have been canceled. With respect to claims 6, 7, 15, and 16 this rejection is respectfully traversed. The examiner states that:

> As for claims 5-6 and 14-15, though Olarig fails to teach his system as a symmetric multi-processor system (SMP) including L3 and L2 cache, Arimilli '115 teaches a processing system with configurable memory bus and scalability



PAGE 17/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

> port which specifically apply to an SMP (see abstract), that includes both L2 and L3 cache (col. 5, lines 46-55 and col. 6, lines 19-34).
>
> As for claims 7 and 16, Olarig fails to teach the processors as being located on multi-chip modules, wherein optimal allocations are based on the location of the processors on the modules.
>
> Arimilli '115 however teaches a system containing SMPs, which are located on multi-chip modules (col. 2, lines 20-42). Arimilli '115 further teaches allocating and connecting the processors on the modules to the cache based on bandwidth utilization. In other words, smaller number of processors can be allocated to particular memory partition if the bandwidth allocation needs to be lower. This way, the memory usage can be optimized based on the location of the modules (i.e. more processors located on a bus that has higher allocation, and less processors located on buses with lower bandwidth allocation) -col. 6, lines 19-35.
>
> It would have been obvious to one of ordinary skill in the art at the time of the invention for Olarig to further include Arimilli's ('115) data processing system to his own system of cache partitioning. By doing so, Olarig would be able to dynamically configure a bus allocation of a processor chip utilizing hardware and software allocation methods, and efficiently allocate processor chip bus bandwidth in order to improve the overall data processing system as taught by Arimilli '115 (col. 3, lines 44-56).

Office Action of March 17, 2006, pp. 9-10.

The examiner has failed to state a *prima facie* obviousness rejection of claims 6, 7, 15, and 16 because the proposed combination, when considered as a whole, does not teach all of the features of these claims. As shown above vis-à-vis the response to the anticipation rejection of claim 1, *Olarig* does not teach any of the claimed features of the independent claims, from which claims 6, 7, 15, and 16 depend. Additionally, *Olarig* does not suggest any of the features of these claims because *Olarig's* teachings deal with partitioning caches and assigning the cache partitions to processors or other entities, not to assigning processors to partitions as claimed in these claims.

Moreover, *Arimilli '115* does not teach or suggest any of the features of the independent claims from which claims 6, 7, 15, and 16 depend. *Arimilli '605* is directed to allocating processor chip I/Os to memory components, I/O components, and other processor chips based on overall system or processor needs. *Arimilli '115* describes dynamically configuring *a bus allocation* of a processor chip utilizing hardware/and or software allocation methods using static and dynamic allocation mechanisms. *Arimilli '115* allocates processor chip ***bus*** bandwidth in such a manner that the efficiency of the processor and the overall data processing system is enhanced.

However, nothing in *Arimilli '115* teaches or suggests assigning processors to partitions, as claimed in the independent claims from which claims 6, 7, 15, and 16 depend. Likewise, nothing in *Arimilli '115*



PAGE 18/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

teaches or suggests that cache usage by the processors is optimized for the cache level, as claimed in the independent claims from which claims 6, 7, 15, and 16 depend.

Because neither *Arimilli '115* nor *Olarig* teach or suggest all of the features of the independent claims from which claims 6, 7, 15, and 16 depend, the proposed combination of *Arimilli '115* and *Olarig*, when considered as a whole, does not teach or suggest all of the features of the independent claims from which claims 6, 7, 15, and 16 depend. Therefore, under the standards of *In re Lowry* and *In re Grabiak*, the examiner has failed to state a *prima facie* obviousness rejection of claims 6, 7, 15, and 16.

**VII.C. Claims 9, 17, and 20**

The examiner rejected claims 9, 17, and 20 under 35 U.S.C. § 103 as obvious over *Olarig* in view of *Mock et al.*, Method and Apparatus for Data Recovery Optimization in a Logically Partitioned Computer System, U.S. Patent Application Publication 2003/0084372 (May 1, 2003) (hereinafter "*Mock*"). The examiner states that:

> As for claims 9 and 17, Olarig fails to teach a memory for storing instructions, which the processors use to carry out the remaining steps of the claim (the remaining steps are discussed under the rejection of claim 1 presented *supra*). Mock however teaches an apparatus for data recovery optimization in a logically partitioned computer system, in which the processors in the multiprocessor system use instructions stored in main memory to carry out their respective functions (paragraph 0034, all lines 1-1 1).
>
> As for claim 20, Olarig teaches removing the partition for the set of partitions in response to allocating a set to the partition (paragraph 0019, all lines - once allocated the partition is no longer available to the remaining processors until the reallocation is determined with the statistical information collected by the system).
>
> It would have been obvious to one of ordinary skill in the art at the time of the invention for Olarig to further include Mock's apparatus for data recovery in a logically partitioned computer system. By doing so, Olarig would benefit by not only having a means of recovering data in his system, but have a system that is capable of implementing a recovery strategy that accurately reflects the current system configuration. This would in turn increase overall system performance, as discussed by Mock in paragraph 0014, all lines.

Office Action of March 17, 2006, pp. 10-11 (emphasis in original).

The examiner has failed to state a *prima facie* obviousness rejection of claims 9, 17, and 20 because the proposed combination, when considered as a whole, does not teach all of the features of these claims. As shown above vis-à-vis the response to the anticipation rejection of claim 1, *Olarig* does not teach any of the claimed features of the independent claims from which claims 6, 7, 15, and 16 depend. Additionally, *Olarig* does not suggest any of the features of these claims because *Olarig's* teachings deal with partitioning



PAGE 19/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

caches and assigning the cache partitions to processors or other entities, not to assigning processors to partitions as claimed in these claims.

Moreover, *Mock* does not teach or suggest any of the features of the independent claims from which claims 6, 7, 15, and 16 depend. *Mock* is directed to a protection utility. The protection utility is for compiled data in a computer system having dynamically configurable logical partitions. The protection utility determines the time for rebuilding compiled data and selectively stores data in a form not requiring rebuild in order to meet a pre-specified recovery time limit. If the configuration changes, the protection utility migrates the protection strategy to adapt to the new configuration.

However, nothing in *Mock* teaches or suggests assigning processors to partitions, as claimed in the independent claims from which claims 6, 7, 15, and 16 depend. Likewise, nothing in *Mock* teaches or suggests that cache usage by the processors is optimized for the cache level, as claimed in the independent claims from which claims 6, 7, 15, and 16 depend.

Because neither *Mock* nor *Olarig* teach or suggest all of the features of the independent claims from which claims 6, 7, 15, and 16 depend, the proposed combination of *Mock* and *Olarig*, when considered as a whole, does not teach or suggest all of the features of the independent claims from which claims 6, 7, 15, and 16 depend. Therefore, under the standards of *In re Lowry* and *In re Grabiak*, the examiner has failed to state a *prima facie* obviousness rejection of claims 9, 17, and 20.

**VII.D. Claims 18 and 19**

The examiner rejected claims 18 and 19 under 35 U.S.C. § 103 as obvious over *Olarig* in view of *Mock* in view of *Arimilli '605*. The rejection of claim 18 is moot as this claim has been canceled. The rejection of claim 19 is respectfully traversed. The examiner states that:

> As for claim 18-1 9, though Olarig teaches his system as including multiple cache levels, he fails to teach repeating the steps of claim 1 for each cache level by moving from the highest cache level, to each successively lower cache level.
>
> Arimilli '605 however teaches a method for controlling eviction of cache blocks to override the eviction of a value, which is reserved for a later operation. More specifically, Arimilli '605 teaches performing system operations on a hierarchical, multilevel cache (i.e. setting an address reservation flag), by starting at the highest cache level (in this case, L2), and then repeating the system operation on the next lower level - col. 3, lines 46-65.
>
> It would have been obvious to one of ordinary skill in the art at the time of the invention for Olarig to further include Arimilli's ('605) system of eviction override into his own system of cache partitioning, in order to facilitate repeating the partitioning/allocation techniques of his memory system on each successive level of cache. By doing so, Olarig would benefit by having a means of improving the overall processor performance of his system by avoiding unnecessary evictions to the cache. This way the overall performance will



PAGE 20/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

> improve by avoiding a scenario in which it is necessary to reload a block that been unnecessarily evicted from the cache memory as taught by Arimilli '605 - col. 7, lines 38-58.

Office Action of March 17, 2006, pp. 11-12.

The examiner has failed to state a *prima facie* obviousness rejection of claim 19 because the proposed combination, when considered as a whole, does not teach all of the features of this claim. As shown above vis-à-vis the response to the anticipation rejection of claim 1, *Olarig* does not teach any of the claimed features of independent claim 17, from which claim 19 depends. Additionally, *Olarig* does not suggest any of the features of these claims because *Olarig's* teachings deal with partitioning caches and assigning the cache partitions to processors or other entities, not to assigning processors to partitions as claimed in these claims.

Moreover, as explained above, *Armilli '605* does not teach or suggest any of the features of claim 17. Similarly, as explained above, *Mock* does not teach or suggest any of the features of claim 17.

Because none of *Olarig*, *Mock*, or *Armilli '605* teach or suggest all of the features of claim 17, the proposed combination of *Olarig*, *Mock*, and *Armilli '605*, when considered as a whole, does not teach or suggest all of the features of claim 17. Therefore, under the standards of *In re Lowry* and *In re Grabiak*, the examiner has failed to state a *prima facie* obviousness rejection of claim 19.

**VII.E. Claims 21-23**

The examiner rejected claims 21-23 under 35 U.S.C. § 103 as obvious over *Olarig* in view of *Mock* in view of *Arimilli '115*. The examiner states that:

> As for claims 21-22, though Olarig fails to teach his system as a symmetric multiprocessor system (SMP) including L3 and L2 cache, Arimilli '1 15 teaches a processing system with configurable memory bus and scalability port which specifically applies to an SMP (see abstract), that includes both L2 and L3 cache (col. 5, lines 46-55 and col. 6, lines 19-34).
>
> As for claim 23, Olarig fails to teach the processors as being located on multichip modules, wherein optimal allocations are based on the location of the processors on the modules.
>
> Arimilli '115 however teaches a system containing SMPs, which are located on multi-chip modules (col. 2, lines 20-42). Arimilli '115 further teaches allocating and connecting the processors on the modules to the cache based on bandwidth utilization. In other words, smaller number of processors can be allocated to particular memory if the bandwidth allocation needs to be lower. This was, the memory usage can be optimized based on the location of the modules (i.e. more processors located on a bus that has higher allocation, and less processors located on buses with lower bandwidth allocation) -col. 6, lines 19-35.



PAGE 21/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

> It would have been obvious to one of ordinary skill in the art at the time of the invention for Olarig to further include Arimilli's ('115) data processing system to his own system of cache partitioning. By doing so, Olarig would be able to dynamically configure a bus allocation of a processor chip utilizing hardware and software allocation methods, and efficiently allocate processor chip bus bandwidth in order to improve the overall data processing system as taught by Arimilli '115 (col. 3, lines 44-56).

Office Action of March 17, 2006, pp. 12-13.

The examiner has failed to state a *prima facie* obviousness rejection of claims 21-23 because the proposed combination, when considered as a whole, does not teach all of the features of these claims. As shown above vis-à-vis the response to the anticipation rejection of claim 1, *Olarig* does not teach any of the claimed features of independent claim 17, from which claims 21-23 depend. Additionally, *Olarig* does not suggest any of the features of these claims because *Olarig's* teachings deal with partitioning caches and assigning the cache partitions to processors or other entities, not to assigning processors to partitions as claimed in these claims.

Moreover, as explained above, *Armilli '115* does not teach or suggest any of the features of claim 17. Similarly, as explained above, *Mock* does not teach or suggest any of the features of claim 17.

Because none of *Olarig*, *Mock*, or *Armilli '115* teach or suggest all of the features of claim 17, the proposed combination of *Olarig*, *Mock*, and *Armilli '115*, when considered as a whole, does not teach or suggest all of the features of claim 17. Therefore, under the standards of *In re Lowry* and *In re Grabiak*, the examiner has failed to state a *prima facie* obviousness rejection of claims 21-23.

**VII.F. All Obviousness Rejections**

With respect to all of the obviousness rejections, the examiner has failed to state *prima facie* obviousness rejections because the examiner has failed to state proper teachings, suggestions, or motivations to combine the references in the manners proposed. As shown above, the examiner's understanding of *Olarig* is backwards. Therefore, all of the proposed motivations make no sense in the context of combining the references to achieve the claimed inventions.

Similarly, the examiner's statements regarding the obviousness of combining the references only state purported advantages of combining the references. An advantage is not necessarily a proper teaching, suggestion, or motivation to combine the references.

To constitute a proper teaching, suggestion, or motivation, the examiner must establish that one of ordinary skill would both recognize the advantage and have a reason to implement the advantage. For example, a first reference may disclose the use of lasers to achieve nuclear fusion. A second reference may disclose that ultra-high power lasers deliver more energy. One of ordinary skill may recognize that an ultra-high power laser would be more useful to achieve nuclear fusion. However, one of ordinary skill



PAGE 22/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50

would be motivated to avoid combining the references because of the extreme expense of ultra-high power lasers. In this example, one of ordinary skill is motivated to avoid implementing the combination, even if he or she recognized the advantage. Therefore, in this example, so no teaching, suggestion, or motivation exists to combine the references.

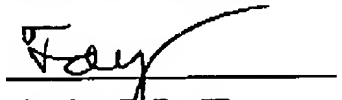
In the case at hand, the examiner has not provided sufficient reasons why one of ordinary skill would recognize the proposed advantages or have reasons to implement them. Therefore, again, the examiner has failed to state *prima facie* obviousness rejections of the claims.

## VIII. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance. The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: June 14, 2006

Respectfully submitted,



Theodore D. Fay III
Reg. No. 48,504
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicant



PAGE 23/23 * RCVD AT 6/14/2006 10:37:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/12 * DNIS:2738300 * CSID:972 385 7766 * DURATION (mm-ss):07-50